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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/699,734	11/04/2003	Takahisa Hayashi	2003-1559A	6435

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EXAMINER	
MANDALA, VICTOR A	
ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 02/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/699,734	HAYASHI, TAKAHISA	
	Examiner	Art Unit	
	Victor A Mandala Jr.	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) *6-11* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/4/03 & 6/14/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Future amended claims are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected Species there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 11/23/04.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3 and 5 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 6,392,265 Kondo et al.

2. Referring to claim 1, a semiconductor device, comprising: a substrate, (Figure 8A #10), including an integrated circuit, (Figure 8A #12); an interlayer insulating layer, (Figure 8A #22), formed on said substrate, (Figure 8A #10); a ferroelectric capacitor, (Figure 8A #70), formed by a first electrode layer, (Figure 8A #64), a ferroelectric layer, (Figure 8A #66), and a second electrode layer, (Figure 8A #68), deposited on said interlayer insulating layer, (Figure 8A #22), in this order; a wiring layer, (Figure 8A #56), electrically connecting said second electrode layer, (Figure 8A #68), of said ferroelectric capacitor, (Figure 8A #70), to said integrated circuit, (Figure 8A #12), through a contact hole, (Figure 8A #24a), in said interlayer insulating layer, (Figure 8A #22); and an insulating side wall film, (Figure 8A #50), covering a peripheral section

of said ferroelectric capacitor, (Figure 8A #70), and being spaced from a peripheral edge section of said contact hole, (Figure 8A #24a).

3. Referring to claim 2, a semiconductor device, wherein said integrated circuit includes a contact plug, (Figure 8A #24a), within said contact hole, (Figure 8A #24a), and said wiring layer, (Figure 8A #56), electrically connects to said contact plug, (Figure 8A #24a).

4. Referring to claim 3, a semiconductor device, wherein said interlayer insulating layer, (Figure 8A #22), includes a plug oxidation protective film consisting of silicon nitride, (Figure 8A #26 & Col. 4 Lines 49-50), and silicon oxide, (Figure 8A #28 & Col. 4 Lines 50-51), and said ferroelectric capacitor, (Figure 8A #70), mounted on said interlayer insulating layer, (Figure 8A #22).

5. Referring to claim 5, a semiconductor device, wherein said ferroelectric layer consists of bismuth strontium tantalate, (Figure 8A #66 & Col. 6 Lines 58-59).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 4, & 5 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 6,249,014 Bailey.

6. Referring to claim 1, a semiconductor device, comprising: a substrate, (Figure 9B #1070), including an integrated circuit, (Figure 9B examiner's label #1); an interlayer insulating layer, (Figure 9B examiner's label #2), formed on said substrate, (Figure 9B #1070); a ferroelectric capacitor, (Figure 9B examiner's label #4), formed by a first electrode layer, (Figure 9B #1078), a ferroelectric layer, (Figure 9B #1080), and a second electrode layer, (Figure 9B #1082), deposited on said interlayer insulating layer, (Figure 9B examiner's label #2), in this order; a wiring layer, (Figure 9B #1092), electrically connecting said second electrode layer, (Figure 9B #1082), of said ferroelectric capacitor, (Figure 9B examiner's label #4), to said integrated circuit, (Figure 9B examiner's label #1), through a contact hole, (Figure 9B examiner's label #3), in said interlayer insulating layer, (Figure 9B examiner's label #2); and an insulating side wall film, (Figure 9B #1086), covering a peripheral section of said ferroelectric capacitor, (Figure 9B examiner's label #4), and being spaced from a peripheral edge section of said contact hole, (Figure 9B examiner's label #3).

7. Referring to claim 2, a semiconductor device, wherein said integrated circuit includes a contact plug, (Figure 9B examiner's label #3), within said contact hole, (Figure 9B examiner's label #3), and said wiring layer, (Figure 9B #1092), electrically connects to said contact plug, (Figure 9B examiner's label #3).

8. Referring to claim 4, a semiconductor device, wherein said insulating sidewall film includes a hydrogen diffusion prevention layer, (Figure 9B #1086).

9. Referring to claim 5, a semiconductor device, wherein said ferroelectric layer consists of bismuth strontium tantalate, (Figure 9B #1080 and Col. 13 Lines 46-52).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Victor A Mandala Jr. whose telephone number is (571) 272-1918. The examiner can normally be reached on Monday through Thursday from 8am till 6pm..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

VAMJ
1/28/05

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